## WHAT IS CLAIMED IS:

1. A method of forming and cleaning a via in a partially fabricated integrated circuit having a top, wherein the integrated circuit comprises a metal layer, an anti-reflective coating above the metal layer, and a dielectric layer above the anti-reflective coating, the method comprising:

depositing an organic resist layer on the top of the partially fabricated integrated circuit;

forming an opening in the resist layer;

etching a via through the opening in the resist layer, wherein the via extends through the dielectric layer and the anti-reflective coating, thereby exposing the metal layer; and

cleaning the via by exposing the via to a plasma that simultaneously removes the resist layer, wherein the plasma is formed from a gas comprising ammonia.

- 2. The method of Claim 1, wherein the gas comprises oxygen.
- 3. The method of Claim 1, wherein the gas comprises at least 25% ammonia.
- 4. The method of Claim 3, wherein the gas comprises at least about 50% ammonia.
- 5. The method of Claim 1, wherein exposing the via to a plasma occurs at a temperature between about 100° and about 400°C.
  - 6. The method of Claim 1, wherein the dielectric layer comprises an oxide.
  - 7. The method of Claim 1, wherein etching a via comprises a plasma etch.
- 8. The method of Claim 1, further comprising depositing a conductive material into the via after cleaning the via.
- 9. A method of forming and cleaning a void in a partially fabricated integrated circuit comprising:

depositing a resist layer on a top of the partially fabricated integrated circuit; forming an aperture in the resist layer;

etching a void through the aperture in the resist layer and through an underlying dielectric layer to expose a metal layer, thereby forming a residue in the void; and

removing the resist layer and the residue from the void by exposing the partially fabricated integrated circuit to a plasma formed from a gas comprising ammonia and rinsing the exposed void.

- 10. The method of Claim 9, wherein the residue comprises metal from the metal layer.
- 11. The method of Claim 9, wherein etching the void comprises performing a directional etch.
- 12. The method of Claim 11, wherein etching the void comprises a reactive ion etch.
- 13. The method of Claim 12, wherein a radio frequency power is set to at least about 900 W during the reactive ion etch.
- 14. The method of Claim 12, wherein the reactive ion etch is magnetically enhanced.
- 15. The method of Claim 9, wherein etching through the mask comprises etching through a metal covering layer situated between the first metal layer and the dielectric layer.
- 16. The method of Claim 15, wherein the metal covering layer comprises an antireflection layer.
- 17. The method of Claim 15, wherein the metal covering layer comprises titanium nitride.
- 18. The method of Claim 9, wherein rinsing the exposed void comprises dipping the integrated circuit into a dilute phosphoric acid bath.
- 19. The method of Claim 9, wherein rinsing the exposed void comprises exposing a void sidewall to deionized water.
- 20. The method of Claim 9, wherein rinsing the exposed void comprises exposing a void sidewall to isopropyl alcohol.